What is claimed is:

1. (Currently Amended) A field effect transistor comprising:

a silicon substrate, wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth;

an epitaxial silicon layer ~~above~~ on said top surface of said silicon substrate; and

a gate stack above said epitaxial silicon layer.

2. (Original) The field effect transistor in claim 1, wherein source/drain and halo dopants are substantially limited to said epitaxial silicon layer.

3. (Original) The field effect transistor in claim 1, wherein said increased oxygen content limits dopants within said epitaxial silicon layer from moving into said silicon substrate.

4. (Original) The field effect transistor in claim 1, wherein said epitaxial silicon layer comprises an in-situ doped epitaxial silicon layer.

5. (Original) The field effect transistor in claim 1, further comprising source/drain regions in said epitaxial silicon layer.

6. (Original) The field effect transistor in claim 1, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

7. (Original) The field effect transistor in claim 1, further comprising sidewall spacers on said gate conductor.

8. (Original) A field effect transistor comprising:

a silicon substrate, wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth;

an epitaxial silicon halo layer on said top of said silicon substrate;

an epitaxial silicon source/drain layer on said epitaxial silicon halo layer; and

a gate stack above said epitaxial silicon source/drain layer.

9. (Original) The field effect transistor in claim 8, wherein source/drain dopants are substantially limited to said epitaxial silicon source/drain layer.

10. (Original) The field effect transistor in claim 8, wherein said increased oxygen content substantially limits dopants within said epitaxial silicon layer from moving into said silicon substrate.

11. (Original) The field effect transistor in claim 8, wherein said silicon substrate includes a column portion extending through said epitaxial silicon panel layer and said epitaxial silicon source/drain layer, wherein said column portion is below said gate conductor.

12. (Original) The field effect transistor in claim 8, wherein halo dopants are substantially limited to said epitaxial silicon halo layer.

13. (Original) The field effect transistor in claim 8, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

14. (Original) The field effect transistor in claim 8, further comprising sidewall spacers on said gate conductor.

15-28. (Cancelled).

29. (New) A field effect transistor comprising:

a silicon substrate, wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth;

an epitaxial silicon source/drain layer on said top of said silicon substrate; and

a gate stack above said epitaxial silicon source/drain layer.

30. (New) The field effect transistor in claim 29, wherein source/drain dopants are substantially limited to said epitaxial silicon source/drain layer.

31. (New) The field effect transistor in claim 29, wherein said increased oxygen content substantially limits dopants within said epitaxial silicon layer from moving into said silicon substrate.

32. (New) The field effect transistor in claim 29, wherein said silicon substrate includes a column portion extending through said epitaxial silicon panel layer and said epitaxial silicon source/drain layer, wherein said column portion is below said gate conductor.

33. (New) The field effect transistor in claim 29, wherein halo dopants are substantially limited to said epitaxial silicon halo layer.

34. (New) The field effect transistor in claim 29, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.